

Memory With 6T Small Aspect Ratio Cells Having Metal\_1 Elements  
Physically Connected to Metal\_0 Elements

ABSTRACT OF THE DISCLOSURE

A method of forming memory circuit (20) comprising a plurality of six transistor memory cells (SC<sub>2</sub>(WL,C)). The method forms each of the six transistor memory cells to comprise a first inverter having an input and an output and a second inverter having an input and an output. The inverters comprise respective first and second drive transistors (DT<sub>1</sub>, DT<sub>2</sub>), each comprising first and second source/drain regions and a gate, and first and second pull-up transistors (PT<sub>1</sub>, PT<sub>2</sub>), each comprising first and second source/drain regions and a gate. The output of the first inverter is coupled to the first source/drain region of the first drive transistor and to the first source/drain region of the first pull up transistor. The output of the second inverter is coupled to the first source/drain region of the second drive transistor and to the first source/drain region of the second pull up transistor. Each cell further comprises a first and second access transistor (AT<sub>1</sub>, AT<sub>2</sub>), each having a gate, and having a first source/drain region coupled to an inverter output and a second source/drain region for communicating to a corresponding bit line. The method 5 also forms at least one insulating layer (128) in a position relative to the first through sixth transistors, and applies a first mask to the at least one insulating layer to form a plurality of vias through the at least one insulating layer. The method also forms a first conducting 10 layer comprising a plurality of conducting plugs (130<sub>x</sub>) in the plurality of vias. The plurality of conducting plugs comprise a first conducting plug (130<sub>4</sub>) coupled to the output of the first inverter and a second conducting plug (130<sub>11</sub>) coupled to the first source/drain region of the first pull-up transistor and to the gate of the second drive transistor and to the gate of the second pull-up transistor. The plurality of conducting plugs further 15 comprise a third conducting plug (130<sub>5</sub>) coupled to the output of the second inverter and a fourth conducting plug (130<sub>12</sub>) coupled to the first source/drain region of the second pull-up transistor and to the gate of the first drive transistor and to the gate of the first pull-up transistor. The method also forms a second conducting layer comprising a plurality of 20 conducting elements (132<sub>x</sub>). The plurality of conducting elements comprise a first 25

conducting element (132<sub>9</sub>) coupled to and physically contacting the first conducting plug and coupled to and physically contacting the second conducting plug and a second 30 conducting element (132<sub>10</sub>) coupled to and physically contacting the third conducting plug and coupled to and physically contacting the fourth conducting plug.